UNITED STATES PATENT AND TRADEMARK OFFICE

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10/814,483	03/31/2004	Gerald L. Dybsetter	15436.366.1	7758

22913   7590   12/26/2007
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EXAMINER
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
 Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _10 December 2007_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-40_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-40_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _31 March 2004_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1.   A request for continued examination under 37 CFR 1.114, including the fee set forth in

37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible

for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has

been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37

CFR 1.114. Applicant's submission filed on December 10, 2007 has been entered.

Claim Rejections - 35 USC § 112

2.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of
> making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the
> art to which it pertains, or with which it is most nearly connected, to make and use the same and shall
> set forth the best mode contemplated by the inventor of carrying out his invention.

3.   Claim 40 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the

written description requirement. The claim(s) contains subject matter which was not described

in the specification in such a way as to reasonably convey to one skilled in the relevant art that

the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 40 recites "interspersing a bit at a guaranteed minimum frequency." This is not supported

by the specification

Claim Rejections - 35 USC § 102

4.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public
> use or on sale in this country, more than one year prior to the date of application for patent in the United
> States.

5.   Claims 1-5, 8-10, 12, 13, 23-26 and 28-30 are rejected under 35 U.S.C. 102(b) as being

anticipated by Creedon et al.(US 6,385,669).

6.   Regarding claim 1, Creedon discloses a system that includes a master

component(Figure 1, 10) that is configured to communicate with one or more slave

components(Figure 1, 11) over a clock wire(Figure 1, 12) and a data wire(Figure 1, 13), a

method for the master component communicating over the data wire while enabling recovery of

synchronization between the master component and the one or more slave components, the

method comprising the following: an act of determining that an operation is to be performed on a

slave component of the one or more slave components(Column 4, Lines 60-61); an act of

monitoring the data wire of the two-wire interface upon determining that the operation is to be

performed on the slave component; an act of detecting at least the predetermined number of

consecutive bits of the same binary polarity have occurred on the data wire during the act of

monitoring the data wire(Column 4, Lines 62-67); and an act of asserting a frame of a two-wire

interface on the data wire in response to the act of detecting that the predetermined number of

consecutive bits of the same polarity have occurred on the data wire(Figure 4; Column 5, Line

7).

7.   Regarding claim 2, Creedon discloses a method, wherein the two-wire interface is a

guaranteed header two-wire interface(Figure 4).

8.   Regarding claim 3, Creedon discloses a method, wherein the two-wire interface is not a

guaranteed header two-wire interface(Column 4, Line 67-Column 5, Line 6).

9.   Regarding claim 4, Creedon discloses a method, wherein the act of detecting at least the

predetermined number of consecutive bits comprises the following: an act of detecting at least

the predetermined number of consecutive bits of a logical one(Column 4, Lines 62-67).

10.   Regarding claim 5, Creedon discloses a method, wherein the data wire is pulled high when no components are asserting binary values on the data wire(Column 4, Lines 43-44).

11.   Regarding claim 8, Creedon discloses a method, further comprising the following: an act of the master component asserting a clock signal on the clock wire during at least some of the act of monitoring the data wire(Column 4, Lines 62-67).

12.   Regarding claim 9, Creedon discloses a method, further comprising the following: an act of the master component asserting a voltage level on the data wire during only a portion of the act of monitoring(Column 4, Lines 62-67).

13.   Regarding claim 10, Creedon discloses a method, wherein the data wire is pulled high when no components are asserting binary values on the data wire(Column 4, Lines 43-44).

14.   Regarding claim 12, Creedon discloses a method, further comprising the following: an act of the master component refraining from asserting a voltage level on the data wire during the act of monitoring(Column 4, Lines 62-67).

15.   Regarding claim 13, Creedon discloses a method, wherein the data wire is pulled high when no components are asserting binary values on the data wire(Column 4, Lines 62-67).

16.   Regarding claim 23, Creedon discloses a system comprising the following: a master component(Figure 1, 10); a slave component(Figure 1, 11); a clock wire(Figure 1, 14) interconnected between the master component and the slave component; a data wire(Figure 1, 13) interconnected between the master component and the slave component, wherein the master component is configured to perform the following: an act of determining that an operation is to be performed on the slave component(Column 4, Lines 60-61); an act of monitoring the data wire of the two-wire interface upon determining that the operation is to be performed on the slave component; an act of detecting at least the predetermined number of consecutive bits of the same binary polarity have occurred on the data wire during the act of

monitoring the data wire(Column 4, Lines 62-67); and an act of asserting a frame of a two-wire

interface on the data wire in response to the act of detecting that the predetermined number of

consecutive bits of the same polarity have occurred on the data wire(Figure 4; Column 5, Line

7).

17.   Regarding claim 24, Creedon discloses a system, wherein the two-wire interface is a

guaranteed header two-wire interface(Figure 4).

18.   Regarding claim 25, Creedon discloses a system, wherein the two-wire interface is not a

guaranteed header two-wire interface(Column 4, Line 67-Column 5, Line 6).

19.   Regarding claim 26, Creedon discloses a system, wherein the data wire is pulled high

when no components are asserting binary values on the data wire(Column 4, Lines 43-44).

20.   Regarding claim 28, Creedon discloses a master component that is configured to do the

following when coupled to a slave component via a clock wire and a data wire: an act of

determining that an operation is to be performed on the slave component; an act of monitoring

the data wire of the two-wire interface upon determining that the operation is to be performed on

the slave component(Column 4, Lines 60-61); an act of detecting at least the predetermined

number of consecutive bits of the same binary polarity have occurred on the data wire during

the act of monitoring the data wire(Column 4, Lines 62-67); and an act of asserting a frame of a

two-wire interface on the data wire in response to the act of detecting that the predetermined

number of consecutive bits of the same polarity have occurred on the data wire(Figure 4;

Column 5, Line 7).

21.   Regarding claim 29, Creedon discloses a master component, wherein the two-wire

interface is a guaranteed header two-wire interface(Figure 4).

22.   Regarding claim 30, Creedon discloses a master component, wherein the two-wire

interface is not a guaranteed header two-wire interface(Column 4, Line 67-Column 5, Line 6).

Claim Rejections - 35 USC § 103

23.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24.   Claims 6, 7, 11, 14-22 and 31-40 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Creedon, in view of what is well known in the art.

25.   Regarding claims 6 and 27, Creedon does not specifically disclose a system and

method, wherein an act of detecting at least the predetermined number of consecutive bits of a

logical zero. However, official notice is being taken that pull-down resistors are well known in the

art and easily replace pull up resistors when a default zero logic is desired instead of logic

one(see Whitney et al.(US2003/0025587)(Paragraph 69)). It would have been obvious to one of

ordinary skill in the art to replace the pull-up resistor with a pull-down resistor so the master can

detect logical zeros as the preamble.

26.   Regarding claim 7, a pull down resistor, as explained above, would pull the data wire low

if no components are asserting binary values(see Whitney et al.(US2003/0025587)(Paragraph

69)).

27.   Regarding claims 11 and 14, Creedon does not specifically disclose a method, wherein

the data wire is pulled low when no components are asserting binary values on the data wire.

However, official notice is being taken that pull-down resistors are well known in the art and

easily replace pull up resistors when a default zero logic is desired instead of logic one(see

Whitney et al.(US2003/0025587)(Paragraph 69)). It would have been obvious to one of ordinary

skill in the art to replace the pull-up resistor with a pull-down resistor so that the data wire is

pulled low when no components are asserting binary values on the data wire.

28.   Regarding claims 15-18 Creedon discloses an MDIO interface but does not specifically

disclose a method, wherein, an act of determining that a read or write operation is to be

performed with an extended or shorter address as compared to other frames communicated

over the data wire. However, official notice is being taken components having different size

addresses in the MDIO interface is well known in the art(see IEEE 802.3 standard, Section 45.1

Overview). It would have been obvious to one of ordinary skill in the art to determine a read or

write operation is to be performed with an extended or shorter address as compared to other

frames since this give the ability to access more device register while retaining logical

compatibility with the MDIO interface defined in Clause 22 of the IEEE 802.3 standard.

29.   Regarding claims 19 and 20, Creedon does not specifically disclose a method, wherein

an act of determining that a read or write operation is to be performed with cyclic redundancy

checking over the data wire. However, official notice is being taken CRC checking is well known

in the art(see CRC definition submitted with this office action). It would have been obvious to

one of ordinary skill in the art to use CRC checking to ensure there are no errors during

transmission.

30.   Regarding claims 21 and 22, Creedon does not specifically disclose a method, wherein

an act of determining that a read or write operation is to be performed with acknowledgements

over the data wire. However, official notice is being taken acknowledgements are well known in

the art(see ACK definition submitted with this office action). It would have been obvious to one

of ordinary skill in the art to use acknowledgements since this would ensure the master and

slave receiving data properly.

31.   Regarding claims 31-39, Creedon does not specifically disclose a master component, wherein the master component is implemented in a laser transmitter/receiver and the various types of laser transmitter/receivers. However, official notice is being taken, that it is well known in the art to use various types of laser transmitter/receivers(see Nelson et al.(US2005/0111845)(Paragraph 78). It would have been obvious to use any types of laser transmitter/receivers to increase compatibility and realize various data rates applicable to each specific situation or environment.

32.   Regarding claim 40, Creedon does not specifically disclose a master component in accordance with Claim 1, further comprising the following: an act of interspersing a bit at a guaranteed minimum frequency among data transmitted on the data wire, wherein the interspersed bit is of a polarity opposite that of the detected predetermined number of consecutive bits. However, official notice is being taken that this is well known in the art as zero-bit insertion. It would have been obvious to one of ordinary skill in the art to use zero stuffing since this will prevent consecutive bits of data being confused with the preamble of consecutive bits.

Response to Arguments

33.   Applicant's arguments filed December 10, 2007 been fully considered but they are not persuasive.

34.   Applicant argues that the master entity 10 of Creedon seems to imply that the master 10 monitors and detects its own preamble and this arrangement is not described anywhere. However, Examiner notes the section referred to by Applicant(Creedon, Column 4, Lines 58-62) does not state the preamble is generated by master entity 10. It simply states the management frame has a preamble. Furthermore, Creedon discloses that the master entity determines the

voltage level of line 13(Column 4, Lines 14-18). Line 13 is connected to a pull up resistor which causes the default logic of Line 13 to be a logic one(Column 4, Lines 43-44). Creedon then states the preamble consists of 32 consecutive logic ones(Column 4, Lines 62-64). Therefore, Creedon discloses the act of monitoring for at least a predetermined number of consecutive bits of the same binary polarity(i.e. Logic one, which is the default logic caused by the pull up resistor).

35.   Examiner also notes that the applicant's specification states "if the master component 110 is not asserting anything on the data wire 132 during the preamble phase, then the data wire should carry a logical one" and "alternatively, even if the master component 110 is asserting a logical one on the data wire during at least some of the preamble, then the data wire 1232 should still be carrying the logical one during the preamble phase," which is applicant's method of monitoring and detecting consecutive bits(Paragraph 42). This is the same as the Creedon's method for monitoring and detecting the consecutive bits.

36.   Applicant further argues that Creedon does not sending a start frame in response to detecting consecutive bits. However, Creedon has a preamble of 32 consecutive bits followed by the start frame(Column 4, Liens 62-64 and Column 5, Line 7). It is implicit that the start frame is in response to detecting consecutive bits since the frame format requires a preamble of 32 consecutive bits.

37.   Therefore Applicant's arguments are not persuasive.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G. Patel whose telephone number is 571-272-3640. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Rinehart H. Mark can be reached on 571-272-3632. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private

PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you

would like assistance from a USPTO Customer Service Representative or access to the

automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nimesh G Patel
Examiner
Art Unit 2111

NP
December 20, 2007

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